IN THE SPECIFICATION:

Please amend the heading on page 1, line 4 as follows:

~~BACKGROUND ART~~ BACKGROUND OF THE INVENTION

Please amend the paragraph beginning on page 1, line 11 as follows:

~~With the progress in~~ In the art of high-resolution lithography, leading-edge semiconductor integrated circuit devices ~~of these days~~ include an enormous number of semiconductor devices on a substrate. In such advanced semiconductor integrated circuit devices, the use of a single interconnection layer is not sufficient for interconnecting the semiconductor devices on the substrate, and it is ~~practiced~~ common to provide a multilayer interconnection structure on the substrate, wherein a multilayer interconnection structure includes a plurality of interconnection layers stacked with each other with intervening interlayer insulating films.

Please amend the paragraph beginning on page 4, line 18 as follows:

Meanwhile, conventional semiconductor ~~device has~~ devices have achieved large integration density and high performance by miniaturizing the design rule. However, the use of strict design ~~rule invites~~ rules invite the problem of increased interconnection resistance and inter-wiring capacitance, and there is emerging a situation in which further improvement of performance is difficult as long as conventional interconnection material is used. Thus, investigations are being made ~~these days~~ with regard to the use of low-resistance Cu for the interconnection material and further with regard to the use of low-dielectric material for the interlayer insulation film so as to reduce the interconnection capacitance.

Please amend the heading on page 6, line 33 as follows:

~~DISCLOSURE~~ SUMMARY OF THE INVENTION

Please amend the heading on page 9, line 8 as follows:

~~BEST MODE FOR IMPLEMENTING~~ DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION